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Claims

[c1] 1. A method for fabricating a thin film transistor (TFT) array substrate, comprising:
providing a substrate;
forming a plurality of scan lines and a plurality of gates electrically connected to said scan lines on the substrate;
simultaneously forming a plurality of first bonding pads and a plurality of second bonding pads over two edges of the substrate, wherein said first bonding pads are electrically connected with said scan lines;
forming a gate dielectric layer over the substrate, for covering said scan lines, said gates, said first bonding pads and said second bonding pads;
forming a plurality of channel layers over said gate dielectric layers of each of said gates;
forming an ohm contact layers on each of said channel layers;
forming a source and a drain on each of the said contact layers;
forming a data line electrically connecting to each of said sources on the gate dielectric layers, wherein a terminal of each of said data lines is extended to each of the second bonding pads, and wherein said gates, each of said

channel layers and each of said sources and each of said drain constitute a of thin film transistor;

forming a mask layer over said gate dielectric layers, wherein said mask layer is disposed over areas corresponding to said first bonding pads and said second bonding pads;

forming a cover layer over said substrate;

forming a patterned photoresist layer over said cover layer, wherein said photoresist layer partially covering over said two edges of the substrate, wherein said photoresist layer comprises a plurality of first openings, a plurality of second openings and a plurality of third openings, wherein said drains are exposed within said first openings, said data lines are exposed within said second openings, and said second bonding pads are exposed within said third openings;

performing an etching process by using the photoresist layer as an etching mask for removing portions of said cover layer and portions of said gate dielectric layers that are not covered by the photoresist layer and exposing a portion of said second bonding pads that are not covered by said photoresist layer; and

forming an electrode material layer over said photoresist layer to form a plurality of pixel electrodes over said photoresist layer, wherein said electrode material layer fills in each of said first openings, said second openings

and said third openings, and wherein said drains are electrically connected with said pixel electrodes via the first openings, said data lines are electrically connected with said second bonding pads via said second openings, said third openings and said electrode material layer.

[c2] 2. The method of claim 1, wherein siad mask layer is formed during the step of forming said source, said drain and said data lines, or during the step of forming said channel layers and said ohm contact layers, or by a combination of said steps thereof.

[c3] 3. The method of claim 2, wherein said mask layer comprises a ring pattern, and covers a pherpheral area over said first bonding pads and said second bonding pads.

[c4] 4. The method of claim 2, wherein said mask layer layer is formed during the step of forming said channel layers and said ohm contact layers, and wherein said mask layer comprises a plurality of openings having rectangular block patterns covering over said two edges of the substrate.

[c5] 5. The method of claim 2, wherein said mask layer is formed during the step of forming said channel layers and said ohm contact layers, wherein said mask layer

comprises a plurality of openings covering the whole substrate, and wherein a portion of said gate dielectric layer covering said first bonding pads and said second bonding pads is exposed within said openings.

[c6] 6. The method of claim 2, wherein said mask layer is formed during the step of forming said channel layers and said ohm contact layers, and in the step of removing said cover layer and said gate dielectric layer that are not covered by the photoresist layer by using the photoresist layer as an etching mask, and removing an upper portion of of said mask layer.

[c7] 7. The method of claim 1, wherein said mask layer comprises a bilayer structure having a top layer and a bottom layer, wherein said top layer is formed during the step of forming said source, said drain and said data lines, and said bottom layer is formed during the step of forming said channel layers and said ohm contact layers.

[c8] 8. The method of claim 1, wherein before the step of forming said ohm contact layers, further comprises a step of forming an etching stop layer over each of said channel layers over each of said gates.

[c9] 9. A thin film transistor (TFT) array substrate, comprising:

a plurality of scan lines disposed on a substrate;
a plurality of first bonding pads disposed on an edge of a surface of the substrate, wherein the first bonding pads are electrically connecteded to the scan lines;
a plurality of second bonding pads disposed on another edge of the surface of the substrate;
a gate dielectric layer disposed on the substrate, wherein a portion of the first bonding pads, and the second bonding pads are exposed by the gate dielectric layer;
a plurality of data lines disposed on the gate dielectric layer, wherein the data lines are extended to the edge of the substrate and are electrically connected to the second bonding pads;
a first mask layer disposed over the gate dielectric layer partially covering the first bonding pads, wherein a remaining portion of the first bonding pads remain exposed;
a second mask layer disposed over the gate dielectric layer partially covering the second bonding pads, wherein a remaining portion of the second bonding pads remain exposed;
a plurality of thin film transistors disposed on the substrate, wherein each of the thin film transistors comprises a gate, a source/drain, a channel layer and an ohm contact layer, each of the gates is electrically connected to each of the scan lines, each of the sources is

electrically connected to each of the data lines, each of the channel layers is disposed on the gate dielectric layer over each of the gates, and each of the ohm contact layers is disposed on each of the channel layers;
a patterned cover layer covering over the thin film transistors and the gate dielectric layers;
a patterned photoresist layer disposed over the cover layer partially covering the two edges of the substrate such that the remaining portion of the two edges of the substrate are exposed; and
a plurality of pixel electrodes disposed on the photoresist layer corresponding to the disposed thin film transistors, wherein each of the pixel electrodes is electrically connected to each of the drains.

[c10] 10. The thin film transistor array substrate of claim 9, wherein a material of the first mask layer and the second mask layer is comprised of same as that of the source/drain and the data lines, or same as that of the channel layers and the ohm contact layers, or a combination thereof.

[c11] 11. The thin film transistor array substrate of claim 9, wherein the first mask layer and the second mask layer are comprised of a bilayer structure having a top layer and a bottom layer, wherein a material of the top layer is same as that of the source/drain and the data lines, and

a material of the bottom layer is same as that of the channel layers and the ohm contact layers.

[c12] 12. The thin film transistor array substrate of claim 9, wherein the first mask layer and the second mask layer comprises a ring pattern, and covers a pherpheral region of the first bonding pads and the second bonding pads.

[c13] 13. The thin film transistor array substrate of claim 9, wherein the first mask layer and the second mask layer are comprised of a material same as that of the channel layers and the ohm contact layers, and the first mask layer and the second mask layer comprises a plurality of openings having rectangular patterns and cover the two edges of the substrate not covered by the photoresist layer, and wherein a portion of the first bonding pads and the second bonding pads are exposed within the openings.

[c14] 14. The thin film transistor array substrate of claim 9, wherein the first mask layer and the second mask layer are comprised of a material same as that of the channel layers and the ohm contact layers, and the first mask layer and the second mask layer are comprised of a single mask layer having a plurality of openings, wherein a portion of the first bonding pads and the second bonding pads are exposed within the openings.

[c15] 15. The thin film transistor array substrate of claim 9, wherein a plurality of first openings is formed in the photoresist layer for exposing the data lines, and a plurality of second openings is formed in the photoresist layer and the gate dielectric layer for exposing the second bonding pads, and an electrode material layer is disposed into each of the first openings and into each of the second openings for electrically connecting the data lines with the second bonding pads.

[c16] 16. The thin film transistor array substrate of claim 9, wherein further comprises forming an etching stop layer over each of the channel layers over each of the gates.

[c17] 17. A thin film transistor (TFT) array substrate, comprising:
a plurality of scan lines disposed on a substrate;
a plurality of first bonding pads disposed over an edge of a surface of the substrate, wherein the first bonding pads are electrically connected to the scan lines;
a plurality of second bonding pads disposed over another edge of a surface of the substrate;
a gate dielectric layer disposed on the substrate, wherein a portion of the first bonding pads and the second bonding pads are exposed by the gate dielectric layer, and a thickness of the gate dielectric layer located over a

peripheral region of the first bonding pads and the second bonding pads is less than a thickness of the gate dielectric layer elsewhere;

a plurality of data lines disposed on the gate dielectric layer, wherein the data lines are extended to the edge of the substrate and are electrically connected to the second bonding pads;

a plurality of thin film transistors disposed on the substrate, each of the thin film transistors comprises a gate, a source/drain, a channel layer and an ohm contact layer, each of the gates is electrically connected to each of the scan lines, each of the sources is electrically connected to each of the data lines, each of the channel layers is disposed on the gate dielectric layer over each of the gates, each of the ohm contact layers is disposed on each of the channel layers;

a patterned cover layer, covering over the thin film transistors and the gate dielectric layers;

a patterned photoresist layer, disposed over the cover layer and partially covering the two edges of the substrate such that the remaining portion over the two edges are exposed; and

a plurality of pixel electrodes, disposed on the photoresist layer corresponding to the disposed thin film transistors, wherein each of the pixel electrodes is electrically connected to each of the drains.

[c18] 18. The thin film transistor array substrate of claim 17, further comprises a first mask layer and a second mask layer disposed over peripheral region of the gate dielectric layers not covered by the photoresist layer covering over the first bonding pads and the second bonding pads respectively, wherein a material of the first mask layer and the second mask layer is same as that of the channel layers and the ohm contact layers.

[c19] 19. The thin film transistor array substrate of claim 18, wherein the first mask layer and the second mask layer comprises a ring pattern.

[c20] 20. The thin film transistor array substrate of claim 18, wherein the first mask layer and the second mask layer comprises a plurality of openings having rectangular patterns, wherein a portion of the first bonding pads and the second bonding pads are exposed within the openings.

[c21] 21. The thin film transistor array substrate of claim 18, wherein the first mask layer and the second mask layer are comprised of a single mask layer having a plurality of openings, wherein a portion of the first bonding pads and the second bonding pads are exposed within the openings.

[c22] 22. The thin film transistor array substrate of claim 17, wherein a plurality of first openings is formed in the photoresist layer for exposing the data lines, and a plurality of second openings is formed in the photoresist layer and the gate dielectric layer for exposing the second bonding pads, and an electrode material layer is formed into each of the first openings and each of the second openings for electrically connecting with the data lines and the second bonding pads.

[c23] 23. The thin film transistor array substrate of claim 17, further comprising a step of forming an etching stop layer over the channel layers over each of the gates.